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<b>Notice of Allowability</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/618,398	REYNERI ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Brian Young	2819	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--**  
 All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the application filed 7/11/03.
2. ☒ The allowed claim(s) is/are 1-26.
3. ☒ The drawings filed on 11 July 2003 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) ☐ All    b) ☐ Some\*    c) ☐ None    of the:
    1. ☐ Certified copies of the priority documents have been received.
    2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.  
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
  6. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
    - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.
    - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

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| <ol style="list-style-type: none"> <li>1. <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)</li> <li>2. <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)</li> <li>3. <input checked="" type="checkbox"/> Information Disclosure Statements (PTO-1449 or PTO/SB/08),<br/>Paper No./Mail Date <u>7/11/03</u></li> <li>4. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit<br/>of Biological Material</li> </ol> | <ol style="list-style-type: none"> <li>5. <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)</li> <li>6. <input type="checkbox"/> Interview Summary (PTO-413),<br/>Paper No./Mail Date _____.</li> <li>7. <input type="checkbox"/> Examiner's Amendment/Comment</li> <li>8. <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance</li> <li>9. <input type="checkbox"/> Other _____.</li> </ol> |
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1. Claims 1-26 are allowed.
2. The following is an examiner's statement of reasons for allowance: the circuit includes an input terminal coupled to receive an analog input signal, a multiple number of sample-and-hold circuits and a multiple number of analog-to-digital (A/D) converters. The input terminal of each of the sample-and-hold circuits is coupled to receive the analog input signal. Each of the A/D converters has an input terminal and an output terminal, where the input terminal is coupled to an output terminal of a corresponding one of the sample-and-hold circuits. In operation, the sample-and-hold circuits sample the analog input signal sequentially and store a multiple number of analog samples at each of the sample-and-hold circuits. The A/D converters convert the analog samples in parallel to generate digital values at the output terminals of each of the A/D converters. An A/D converter of this type has not been shown in the prior art.
3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."
4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kobatake discloses a high speed and high accuracy A/D converter. A reference voltage generation circuit is provided for dividing a reference voltage into a plurality of divided reference voltages having voltage levels different from each other. A plurality of comparators are provided, each of which has a first input terminal connected to an analog input line for fetching

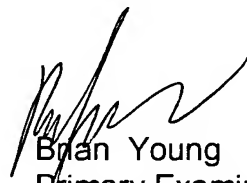
analog signals and a second input terminal connected to the reference voltage generation circuit for fetching a corresponding one of the divided reference voltages so as to compare the analog signals with the divided reference voltage.

Glass et al. disclose a ultra high speed, low power, flash A/D converter utilizing a current mode regenerative comparator method and apparatus for performing analog to digital conversion. A voltage to current converter converts an analog input voltage to an input current. A current reference generates a reference current. A plurality of scaling elements scaled the reference current to yield a plurality of scaled reference currents each corresponding to some voltage level within the dynamic range of the input voltage. The input current is compared to each of the scaled reference currents in a plurality of current comparators to generate a thermometer code from which a digital representation of the analog input voltage is derived.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Young whose telephone number is 571-272-1816. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Brian Young  
Primary Examiner  
Art Unit 2819

bky